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10/511,514	10/14/2004	Francesco Pessolano	NL02 0312 US	4656

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EXAMINER	
MITCHELL, JASON D	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/511,514	PESSOLANO, FRANCESCO	
	Examiner	Art Unit	
	JASON MITCHELL	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to an amendment filed on 6/11/09.

Claims 1-2 and 4-25 are pending in this application.

Response to Arguments

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Applicant's arguments filed 6/11/09 have been fully considered but they are not persuasive in view of the newly cited prior art references. To the extent the rejection has not been changed the applicant's arguments are addressed below.

In the last par. on pg. 14, the applicant states:

> It is respectfully submitted that column 15, lines 19-23 of Trimberger merely discloses that the most commonly used sequences are collected into separate groups, where each group forms a single RISA instruction that performs the whole task. Such a disclosure has nothing to do with allocation between a processing resource and a repeated sub-sequence, let alone performing such an allocation based on the index information, as recited in independent claims 1 and 12.

The examiner respectfully disagrees. col. 15, lines 14-23 reads:

> Thus, techniques for deciding which instructions to configure into the RISA are provided. For instance, the program can be designed to run on the fixed execution unit only, and measurements made of which instructions or instruction sequences are most common. As mentioned above, this measurement technique is called profiling. These most commonly used sequences, which may be bounded by size to manage development of the RISAs, are collected into separate groups. Each group is optimized to form a single RISA instruction that performs the whole task.

Accordingly it should be seen that Trimberger discloses determining an allocation ("deciding which instructions to configure into the RISA") between a processing resource ("RISAs") and a repeated sub sequence ("the most commonly used sequences") based on index information ("the most commonly used").

Starting in the first partial par. on pg. 16, the applicant states:

> ... An index information that comprises an integer number set in proportion with a ranking of the repetition rate, is nowhere disclosed or suggested in Trimberger, and any conclusion otherwise can only be arrived at using impermissible hindsight. Without using the present application as a road map to reconstruct the present invention, and without the benefit of impermissible hindsight, one skilled in the art would not arrive in an obvious manner to having index information that comprises an integer number set in proportion with a ranking of the repetition rate, as recited in independent claims 1, 12, and 18 from the disclosure of Trimberger.

The examiner respectfully disagrees. As the applicant has acknowledged Trimberger discloses ranking the use of sequences from most used to least used (see e.g. col. 15, lines 15-18 and 39-44). Using integer indexes to represent such a ranking (e.g. 1st most used 2nd most used ... Nth most used) would have been within the knowledge and abilities of those of ordinary skill in the art and is a basic and intuitive way to represent such a ranking. Those of ordinary skill in the art would not have needed to refer to the applicant's disclosure for such an implementation.

In the par. bridging pp. 17-18 the applicant states:

> For example, claim 4 recites that "said allocation is determined by comparing said integer number with the number of available processing resources." ... These features are nowhere disclosed or suggested in Trimberger. Rather, column 15, lines 39-44 of Trimberger, cited on page of the Final Office Action in rejecting claim 4, merely recites that the "least used RISA instructions are converted back into fixed

> instructions, or to a combination of fixed instructions and simpler RISA instructions, until the used RISA instructions fit within the available configurable resources." ... Converting RISA instructions back into fixed or simpler instructions until the used RISA instructions fit within the available configurable resources has nothing to do with determining allocation by comparing the integer number set in proportion with a ranking of the repetition rate with the number of available processing resources, as recited in claim 4.

The examiner respectfully disagrees. By removing RISA instructions "until the used RISA instructions fit within the available configurable resources" (col. 15, lines 39-44) Trimberger is disclosing a comparison between the number of sequences and the number of available RISAs (i.e. 8 instructions will not fit in 6 RISAs because '8>6'). Further Trimberger discloses this comparison is based on the disclosed index (i.e. col. 15, lines 39-44 "instructions [sequences] which are used least often"). While Trimberger does not explicitly disclose representing the index as an integer value this modification would have been obvious as discussed above.

In the par. bridging pp. 18-19, the applicant states:

> In addition, the recitation on column 15, line 19-23 of Trimberger, cited in rejection claim 6 on page 8 of the Final Office Action that the "most commonly used sequences, which may be bounded by size to manage development of the RISAs, are collected into separate groups," merely discloses that the most commonly used sequences are collected in a groups that have a maximum size or are "bounded by size to manage development of the RISAs." ... The disclosure that a group has a maximum size does not disclose or suggest that "said index information comprises an information indicating the number of instructions in said repeated sub-sequence," as recited in claim 6. ...

The examiner respectfully disagrees. Trimberger discloses using the number of instructions in a sequence, but does not explicitly disclose how this value is implemented (e.g. stored or retrieved). As noted in the rejection it would have been

obvious and would not have produced any unexpected results to implement this value as part of an 'index' data structure.

Starting in the first full par. on pg. 19 the applicant states:

> Further, in rejecting claim 7 and 21, on pages 8-9 of the Final Office Action, column 15, lines 39-42 of Trimberger is cited which merely disclose finding the least often used RISA instructions and converting them "back into fixed instructions, or to a combination of fixed instructions and simpler RISA instructions, until the used RISA instructions fit within the available configurable resources." (Column 15, lines 41-44) It is respectfully submitted that converting RISA instructions back to fixed or simpler RISA instruction does not disclose or suggest deleting such instructions. There is simply no disclosure or suggestion in Trimberger of "generating an instruction for deleting said repeated sub-sequence," as recited in claim 7.
> Even if assuming, arguendo, that deleting is equivalent to converting back, ... Trimberger is completely silent about resetting anything. Further, there is nothing in Trimberger about forming or converting RISA instructions, regardless of whether that sub-sequence is allocated to any particular processing unit, that discloses or suggests the features or claim 21 to add an instruction to an output sequence that indicates a repeated subsequence is not used anymore.

The examiner respectfully disagrees. By disclosing conversion of RISA instructions back to fixed instructions (see col. 15, lines 39-42) Trimberger disclose removing the converted sub-sequence of instructions from the RISA. Because the instructions are removed they no longer exist on the RISA and thus meet the "deleted" language of the claims (i.e. they have been 'deleted' from the RISA).

Further, specifically regarding claim 21, it is noted that the 'output sequence' is not the same as a 'repeated sequence'. The output sequence refers to the entire set of instructions used to control the system (also note that claim 7 only recites generation of the instruction). Accordingly it is at least necessary to insert an instruction into Trimberger's output sequence to indicate a RISA instruction is not sufficiently used and

should be removed (see e.g. col. 15, lines 44-48 "The compiler relies on these dynamic strategies for optimizing configurable resources" and col. 13, lines 47-49 "reconfiguration of the RISAs may be initiated on command from a running program"). In other words instructions to control the system (e.g. loading and unloading of RISAs) must be included in the program as a whole.

In the par. bridging pp. 21-22, the applicant states:

> Further, as correctly noted on page li of the Final Office Action, Trimberger does not disclose or suggest the apparatus is a digital signal processor (DSP). However, Official Notice is taken that it would have been known to use a DSP for an apparatus that processes information based on a sequence of instructions including providing an index information indicating the repetition frequency of a repeated sub-sequence. Applicant respectfully traverses and requests that the Examiner provide prior art references clearly illustrating that it is well known to provide such a DSP in the context of the claimed combination or some other legally cognizable basis for why the fact that DSPs existed renders the claim combination obvious.

The examiner respectfully notes the applicant has not specifically pointed out the supposed errors in the rejection by stating why the noticed fact is not considered to by common knowledge or well-known in the art and thus has not presented an adequate traversal of the rejection. Accordingly no additional documentary evidence is provided. Further Trimberger discloses using an FPGA (see e.g. col. 10, lines 5-10 "a RISA field programmable gate array (RISA FPGA) 120"). Those of ordinary skill in the art would have recognized FPGA's and DSP's as broadly interchangeable / combinable. (see e.g. applicant's pg. 5, lines 9-16 "Se-DSP 10 comprises a plurality of ports to which processing resources 20 to 23 can be connected ... processing resources ... may be configurable logic blocks, i.e. Field Programmable Gate Arrays (FPGAs)").

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 12-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim elements "detecting means for detecting a repeated sub-sequence" (claim 12, line 4), and "resource control means" (claim 12, line 11) are means (or step) plus function limitations that invoke 35 U.S.C. 112, sixth paragraph. However, the written description fails to disclose the corresponding structure, material, or acts for the claimed function.

"detecting means for detecting a repeated sub-sequence": The specification discloses this detection is preformed (e.g. The compiler is arranged to identify repeated sequences of instructions") but does not disclose how or by what specific structure this detection is preformed. Note that for a computer-implemented means-plus-function claim the corresponding structure for a computer-implemented function must include the algorithm as well as the general purpose computer or microprocessor (see e.g. *Aristocrat Technologies, Inc. v. International Game Technology*, 521 F.3d 1328, 1333, 86 USPQ2d 1235, 1239-40 (Fed. Cir. 2008) and *WMS Gaming, Inc. v. International Game Technology*, 184 F.3d 1339, 51 USPQ2d 1385 (Fed. Cir. 1999))

"resource control means for allocating said repeated sub-sequence": the specification discloses the allocation takes place but does not disclose how or by what specific structure it is preformed.

Applicant is required to:

(a) Amend the claim so that the claim limitation will no longer be a means (or step) plus function limitation under 35 U.S.C. 112, sixth paragraph; or

(b) Amend the written description of the specification such that it expressly recites what structure, material, or acts perform the claimed function without introducing any new matter (35 U.S.C. 132(a)).

If applicant is of the opinion that the written description of the specification already implicitly or inherently discloses the corresponding structure, material, or acts so that one of ordinary skill in the art would recognize what structure, material, or acts perform the claimed function, applicant is required to clarify the record by either:

(a) Amending the written description of the specification such that it expressly recites the corresponding structure, material, or acts for performing the claimed function and clearly links or associates the structure, material, or acts to the claimed function, without introducing any new matter (35 U.S.C. 132(a)); or

(b) Stating on the record what the corresponding structure, material, or acts, which are implicitly or inherently set forth in the written description of the specification, perform the claimed function. For more information, see 37 CFR 1.75(d) and MPEP §§ 608.01(o) and 2181.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-6, 8, 11-14, 16, 18 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,752,035 to Trimberger (Trimberger).

Regarding Claim 1, 12 and 18: Trimberger discloses a method for processing an information based on a sequence of instructions in an apparatus for data processing, said method comprising the steps of:

detecting a repeated sub-sequence in said sequence of instructions by the apparatus for data processing (col. 14, lines 65-67 identifies commonly used sequences of fixed instructions");

providing an index information indicating the repetition frequency of said repeated sub-sequence (col. 15, lines 15-18 "measurements made of which instructions or instruction sequences are most common"), wherein said index information is set in proportion with a ranking of said repetition rate of said repeated sub-sequence compared to the repetition rate of other detected repeated sub-sequences (col. 15, lines 15-18 "which ... sequences are most common"; col. 15, lines 29-41 "instructions which are used least often"; note that the broadly claimed "providing an index information" is at least implicitly taught by Trimberger's ordering of the sequences); and

determining an allocation between a processing resource and said repeated sub-sequence based on said index information (col. 15, lines 19-23 "These most commonly used sequences ... optimized to form a single RSIA instruction that performs the whole task").

Trimberger does not explicitly disclose this ranking comprises an integer number.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to indicate Trimberger's ranking (col. 15, lines 39-44 "least used RISA instructions") with an integer number set in proportion with the ranking (e.g. 1^{st}, 2^{nd}, 3^{rd}, ... N^{th} most used). Those of ordinary skill in the art would have been motivated to do so as a means of indicating the disclosed ranking (col. 15, lines 15-18 "which ... sequences are most common"; col. 15, lines 29-41 "instructions which are used least often"), and because of the ease of storage and manipulation (e.g. comparison) provided by the integer type.

Regarding Claim 4: The rejection of claim 1 is incorporated; further Trimberger discloses said allocation is determined by comparing said ranking with the number of available processing resources (col. 15, lines 39-44 "until the used RISA instructions fit within the available configurable resources.").

Regarding Claim 5: The rejection of claim 4 is incorporated; further Trimberger discloses all repeated sub-sequences for which said integer number is smaller than said number of available processing resources are allocated to a selected processing resource (col. 15, lines 39-44 "until the used RISA instructions fit within the available configurable resources.").

Regarding Claim 6: The rejection of claim 1 is incorporated; further Trimberger discloses determining the number of instructions in a repeated sub-sequence (col. 15, lines 19-23 "commonly used sequences ... bounded by size").

Trimberger does not disclose including the information in said index information.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the number of instructions in a repeated sub-sequence (col. 15, lines 19-23 "sequences ... bounded by size") in said index information. Those of ordinary skill in the art would have been motivated to do so in order to consolidate the profiling information for easy access in determining if the repeated sub-sequence will fit in a RISA unit (col. 15, lines 39-44 "until the used RISA instructions fit within the available configurable resources."). Such a combination would be well within the ordinary level of skill in the art and would have caused nothing but the expected results.

Regarding Claims 8 and 22: The rejections of claims 1 and 18 are incorporated respectively; further Trimberger discloses generating an instruction for specifying processing registers used by said repeated sub-sequence, and using said instruction for locking said specified processing registers (col. 11, lines 1-4 "registers are ... controlled by the RISA FPGA 120 as necessary").

Regarding Claims 11 and 16: The rejections of claims 1 and 13 are incorporated respectively; further Trimberger discloses signaling the presence of external processing units to a central processing unit, and counting the number of available external processing units based on said signaling (col. 14, lines 40-42 "object code is optimized to fit the available configurable resources"; this necessarily requires the claimed counting the number of available external processing units at any given point in the execution).

Regarding Claim 13: The rejection of claim 12 is incorporated; further Trimberger discloses connecting means for connecting at least one external processing unit to which said repeated sub-sequence can be allocated (Fig. 1, 22).

Regarding Claim 14: The rejection of claim 13 is incorporated; further Trimberger discloses a memory table for storing an allocation information indicating an allocation between said at least one external processing unit and corresponding repeated sub-

sequences (col. 7, line 66-col. 8, line 3 "The configuration store 31 may [be] accessible ... for dynamically reprogramming in a field programmable gate array 30").

Regarding Claim 23: The rejection of claim 18 is incorporated; further Trimberger discloses determining the ranking of repeated sub-sequences based on their repetition rate (col. 15, lines 15-18 "which ... sequences are most common"; col. 15, lines 29-41 "instructions which are used least often").

Claims 2, 9-10, 17, 19-20 and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,752,035 to Trimberger (Trimberger) in view of US 5,696,956 to Razdan et al. (Razdan).

Regarding Claims 2, 17 and 19: The rejections of claims 1 and 13 are incorporated appropriately; further Trimberger discloses generating an instruction, and adding said instruction to said sequence of instructions (col. 15, lines 19-23 "form a single RSIA instruction that performs the whole task"; col. 6, lines 19-23 "The identified sequence is replaced in the preliminary object code with a programmed instruction to produce the executable version"; figs 3-5 instructions 201, 256 and PGM OPCODE 274).

Trimberger does not explicitly disclose the instruction containing integer index information.

Razdan teaches an instruction (col. 4, lines 39-43 "the EXPFU Opcode … to identify the instruction as one associated with the PFU") containing integer index information (col. 4, lines 51-59 "The LPnum field is basically an identifier corresponding to an available programming configuration for the PFU") used to determine allocation of the instruction to a processing resource (col. 4, lines 60-66 "the LPnum of the instruction is compared against the currently stored Pnum in the PFU 24").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to generate an instruction (Trimberger col. 6, lines 19-23 "a programmed instruction "; Figs 3-5) including integer index information (Razdan col. 4, lines 51-59 "The LPnum field") representing a frequency of execution of the replaced sub-sequence of instructions (Trimberger col. 15, lines 19-23 "These most commonly used sequences … optimized to form a single RSIA instruction that performs the whole task"). Those of ordinary skill in the art would have been motivated to do so as a known method of implementing the disclosed functionality (Trimberger col. 15, lines 19-23 "These most commonly used sequences … optimized to form a single RSIA instruction that performs the whole task"; Razdan col. 4, lines 51-59 "The LPnum field is basically an identifier corresponding to an available programming configuration for the PFU") which would have provided an efficient means of identifying and executing the "most common instructions" with the RSIA's which would have produced only the expected results (Razdan col. 4, lines 60-66 "the LPnum of the instruction is compared against the

currently stored Pnum in the PFU 24. If there is a match, the EXPFU instruction executes normally").

Regarding Claim 9: The rejection of claim 2 is incorporated; further Trimberger discloses activating a processing resource (20-2n) when said instruction containing said index information indicates that the corresponding repeated sub-sequence has already been allocated to said processing resource (col. 7, line 66-col. 8, line 3 "The configuration store 31 may [be] accessible ... for dynamically reprogramming in a field programmable gate array 30").

Regarding Claim 10: The rejection of claim 9 is incorporated; further Trimberger discloses said activating comprises programming said processing resource according to said corresponding repeated sub-sequence, or uploading said corresponding repeated sub-sequence to a memory of said processing resource (col. 7, line 66-col. 8, line 3 "The configuration store 31 may [be] accessible ... for dynamically reprogramming in a field programmable gate array 30").

Regarding Claim 20: The rejection of claim 19 is incorporated; further Trimberger discloses additional instruction is added so as to proceed said repeated sub-sequence (col. 13, lines 30-33 "The programmed instruction is then executed upon detection of an access to the start of the sequence in the cache, or the program can be re-compiled to include the new programmed instruction").

Regarding Claim 24: The rejection of claim 19 is incorporated further Trimberger discloses said compiler is arranged to allocate said repeated sub-sequence to a separate processing unit (col. 15, lines 19-23 "form a single RSIA instruction that performs the whole task").

Regarding Claim 25: The rejection of claim 19 is incorporated; further Trimberger discloses said compiler is arranged to add an additional instruction to said repeated sub-sequence for use in processing notification at execution time (col. 15, lines 19-23 "form a single RSIA instruction that performs the whole task").

Claim 7 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,752,035 to Trimberger (Trimberger) in view of US 6,327,704 to Mattson et al. (Mattson).

Regarding Claims 7 and 21: The rejection of claim 1 is incorporated accordingly; further Trimberger teaches generating an instruction for deleting said repeated sub-sequence, if said repeated sub-sequence is infrequently executed, and resetting a processing unit to which said deleted repeated sub-sequence was allocated (col. 15, lines 39-42 "instructions which are used least often ... are converted back into fixed instructions").

Trimberger does not disclose that the time period is predetermined.

Mattson teaches determining frequency of a sub-sequence based on a number of executions in a predetermined time period (col. 4, lines 49-53 "is frequently executed when it is executed more than a predetermined number of times in a predetermined interval").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to identify Trimberger's "instructions which are used least often" (col. 15, lines 39-42) as taught by Mattson (col. 4, lines 49-53 "is [in]frequently executed when it is executed [less] than a predetermined number of times in a predetermined interval"; emphasis added to highlight the use in this combination). Those of ordinary skill in the art would have been motivated to do so as a known alternate method of identifying infrequently used instruction sub-sequences which would have produced only the expected results.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,752,035 to Trimberger (Trimberger) in view of Official Notice.

Regarding Claim 15: The rejection of claim 13 is incorporated; further Trimberger discloses, wherein said apparatus is a processor (Fig. 1, 24) and said at least one

external processing units are processor cores and/or configurable logic blocks (Fig. 1, 30).

Trimberger does not disclose the fixed processor is a DSP.

Official notice is taken that DSP's were known and used in the art at the time of invention.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement Trimberger's processor as a DSP. Those of ordinary skill in the art would have been motivated to do so as a known means of implementing the disclosed functionality (Fig. 1, Fixed E-UNIT 24).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON MITCHELL whose telephone number is (571)272-3728. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bullock Lewis can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason Mitchell/
Examiner, Art Unit 2193